Schottky diodes in 40nm bulk CMOS for 1310nm high-speed optical receivers

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Abstract: In this paper, the use of Schottky diodes in CMOS as 1310nm photodetectors is proposed. In contrast with regular pn-diodes, these diodes can convert photons with a wavelength longer than 1.1µm to a high bandwidth current through internal photo emission. Distributed layout n-well and p-well Schottky diodes have been fabricated and characterized in 40nm bulk CMOS. The measured 1310nm DC responsivity for the n-well and p-well Schottky diodes is 0.4mA/W and 0.35A/W respectively for 1V reverse bias. To the authors' knowledge, this is the first 1310nm CMOS photodetector reported.

1. Introduction

Integrating every building block of high-speed optical receivers on a single silicon chip provides an attractive solution regarding cost, size, parasitics, etc. However, silicon is not very well suited for optical conversion due to its relatively wide and indirect band gap. Up to now, every reported integrated CMOS receiver makes use of a pn-photodiode, which implies that the wavelength cannot exceed 1.1µm. On top of that, the bandwidth of the generated photocurrent is very low (1-10MHz), due to slowly diffusing carriers in the substrate [1]. Nevertheless, CMOS integrated 850nm receivers have been demonstrated to achieve bit rates up to 10Gbps using techniques such as such as spatially modulated light detectors and equalizers [2,3]. These techniques require extra power consumption though and ultimately these CMOS optical receivers are not suitable for the typical 1310/1550nm long-haul communication bands.

In this work, an alternative photodetector in the form of Schottky diodes is presented. Although CMOS processes are not conceived to integrate such devices, Schottky diodes have been successfully integrated in 0.13µm CMOS processes for RF-applications [4,5]. Additionally, through the mechanism of internal photo emission (IPE), light with wavelengths above 1.1µm can be detected [6]. The generated current has a much higher intrinsic bandwidth (10-100GHz) [7], relieving the need for an equalizer.

2. CMOS Schottky photodiodes

Being a metal-semiconductor junction, Schottky diodes can be realized in a CMOS process using contacts to lowly doped silicon. If the silicon were heavily doped, the resulting barrier would be so thin that carriers could easily tunnel through it, resulting in an ohmic contact. In this 40nm CMOS chip, 2 Schottky diodes were fabricated, one making use of contacts to a n-well, the other contacts to a p-well. In **Fig. 1** the chip photograph containing the Schottky diodes is shown as well as a top-view and cross-section illustration of the layout of the diodes.

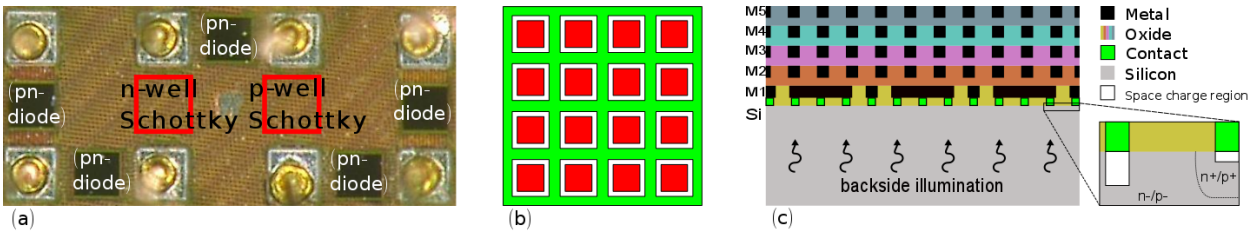

Fig. 1: (a) chip photograph; (b) top-view Schottky distributed layout illustration. Red color denotes Schottky contacts, green color Ohmic contacts; (c) cross-section Schottky layout illustration.

Because the diodes are illuminated from the backside of the chip, no metal dummy blockers were put above the Schottky diodes, rendering them invisible on the chip photograph. The diodes have a dimension of 67.6x67.6µm² in order to receive all the light from a multi-mode fiber, which typically has a core diameter between 50-60µm. Each diode consists of 225 Schottky regions (red in **Fig. 1**b), each containing 256 Schottky contacts. The design rules (minimal contact size and spacing) and the distributed layout lead to a fill factor of 3.7%. This distributed layout has been chosen to keep the series resistance Rs of the diode sufficiently small (see next section).

When light is absorbed in the metal of a Schottky diode, internal photoemission (IPE) occurs. If electrons (holes) are excited to a sufficiently high (low) energy level, they can cross the n-type (p-type) Schottky barrier, resulting in photocurrent. The higher the difference between photon energy and barrier height, the higher the quantum efficiency [6]. When the diodes are illuminated from the backside, the excited carriers are closer to the barrier than is the case for frontside illumination, resulting in higher responsivity. Furthermore, this way, the light only has to cross one layer, namely the silicon substrate, whereas it has to cross the entire dielectric stack when frontside illumination is applied, which could result in additional reflective losses [8]. As already mentioned, through IPE, a larger light spectrum can be converted to a high-speed photocurrent compared to pn-diodes.

3. Proposed optical receiver and advantages

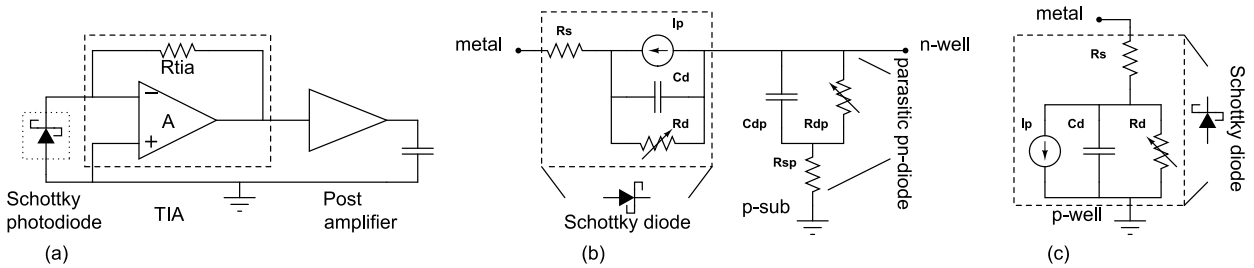

Fig. 2: (a) Circuit diagram of Schottky diode based optical receiver; (b) equivalent schematic of n-well Schottky diode; (c) equivalent schematic of p-well Schottky diode.

A circuit diagram of a 1310nm CMOS optical receiver is shown in **Fig. 2** together with the equivalent schematics of both presented Schottky diodes. Since p-regions in CMOS are grounded, the n-type diode has two available terminals whereas the p-type only has one. The equivalent schematic is paramount for the design of the transimpedance amplifier (TIA) converting the photocurrent into a voltage, to achieve an optimal signal-to-noise ratio [8]. However, since standard CMOS processes are not intended to realize Schottky diodes, there is no documentation or modelling whatsoever available beforehand. In order to design a fully integrated optical receiver based on such a diode, these parameters must first be determined experimentally. In the next section, the values of this equivalent circuit are shown.

4. Measurement results and discussion

Using a Keithley 2450 SourceMeter, the I-V characteristics were obtained at room temperature. They can be seen in **Fig. 3**a. For both diodes, the current does not saturate for increasing reverse voltages. This can be explained by the barrier lowering theory [5], which predicts that the barrier height decreases for increasing reverse voltages. The p-well diode conducts far more current than the n-well diode. This implies that its barrier is lower than that of the n-well diode. After fitting these curves on thermionic current theory, the zero-bias barrier heights of the n-well and p-well diodes are found to be 0.55V and 0.23V respectively. The I-V characteristics also reveal Rd and Rs. Rs can be extracted from the linear behavior at high forward biasing voltages, as Rd is negligible in that region. Rs is found to be approximately 2Ω for both diodes. The non-linear Rd can be found by dividing the junction voltage by the diode current as seen in **Fig. 3**b.

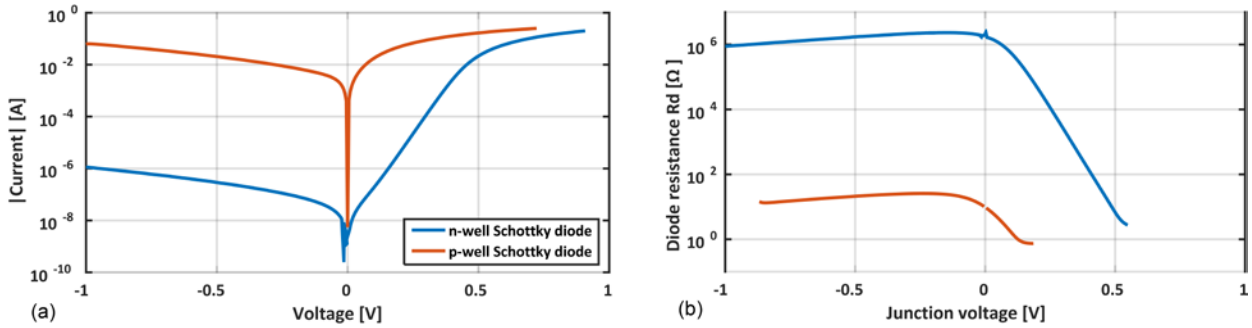

Fig. 3: (a) Measured IV-characteristics; (b) Extracted diode resistance Rd

The diode impedance can be extracted from S-parameters which were measured using a HP 8753C VNA. For this setup, the chip was bonded on a PCB containing 50Ω transmission lines by making use of wire bonding.

The magnitude of the extracted impedances are shown in **Fig. 4**a for different reverse biasing voltages. The n-well diode shows a clear capacitive behavior for moderate frequencies. This is to be expected, since Rd is large in the reverse region and the equivalent impedance is dominated by Cd. At higher frequencies, parasitic inductances, such as the bond wire inductance, become visible. Cd ranges between 4pF and 6.3pF for voltages between -1V and 0V. In the case of the p-well diode, Rd dominates the equivalent impedance for moderate frequencies due to the low barrier height. Parasitic inductances already come into play at frequencies lower than $1/2\pi RdCd$, so this capacitance can not be extracted from the impedance.

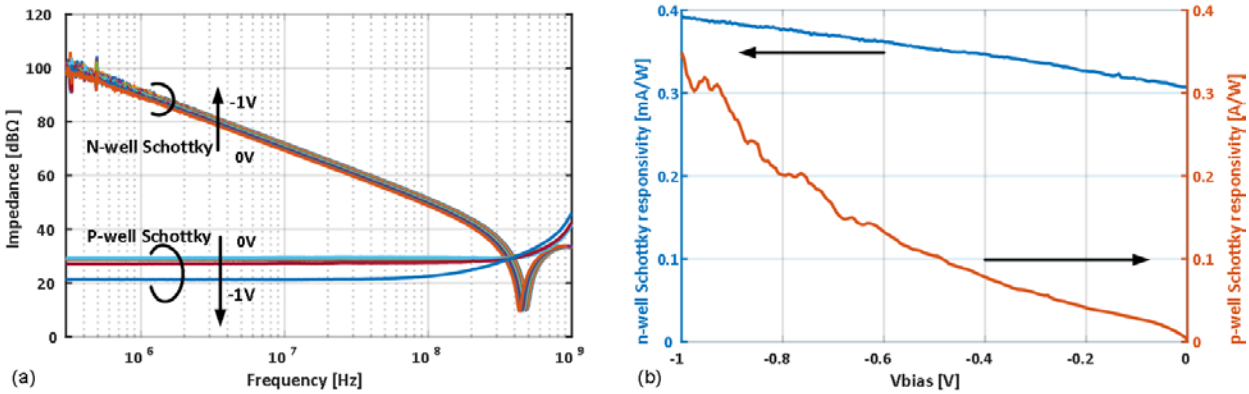

Fig. 4: (a) Extracted diode impedance; (b) Measured 1310nm DC responsivity

In order to perform BSI, the chip was mounted on a PCB by making use of flip-chip bonding. 1310nm laser light was sent trough a multi-mode fiber. The end of the fiber was connected to a lens, of which the spot size is identical to the fiber core diameter (50µm) at the focal length. For a fixed optical power of 1mW, the diode current was measured for different biasing voltages using the Keithley 2450 SourceMeter. The optical power was verified using a Thorlabs S120C power sensor. The results can be seen in **Fig. 4**b. The responsivity increases for increasing reverse biasing voltages. Since the barrier height lowers, the quantum efficiency, and thus the responsivity, increases. The n-well Schottky diode has a 1310nm responsivity of 0.4mA/W for a reverse biasing voltage of 1V. The responsivity of the p-well Schottky diode is 0.35A/W for 1V reverse voltage. This responsivity is much higher due to the low barrier height.

5. Conclusion

This paper demonstrates 1310nm light can be converted to an electrical current in a CMOS process through Schottky diodes. A 40nm chip containing such devices has been fabricated and measured. Theory predicts this current has a very high bandwidth. These diodes enable fully integrated CMOS 1310nm optical receiver without the need of an equalizer and are the first 1310nm photodetectors in CMOS reported to the authors' knowledge.

6. References

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